ABSTRACT

A fractional-type phase-locked loop circuit is proposed for synthesising an output signal multiplying a frequency of a reference signal by a fractional conversion factor, the circuit including means for generating a modulation value, means for generating a feedback signal dividing the frequency of the output signal by a dividing ratio, the dividing ratio being modulated according to the modulation value for providing the conversion factor on the average, means for generating a control signal indicative of a phase difference between the reference signal and the feedback signal, means for controlling the frequency of the output signal according to the control signal, and means for compensating a phase error caused by the modulation of the dividing ratio; in the circuit of an embodiment of the invention, the means for compensating includes means for calculating an incremental value, indicative of an incremental phase error, according to the conversion factor and the modulation value, means for calculating a correction value accumulating the incremental value, and means for conditioning the control signal according to the correction value.